LISTING OF THE CLAIMS

Claim 1 (Original): A method for multiplexing signals comprising:

providing a plurality of select signals and a plurality of input signals for input by a multiplexer, each select signal adapted to cause the multiplexer to select a different one of the plurality of input signals for output by the multiplexer when the select signal is in a first logic state; and

preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state.

Claim 2 (Original): The method of claim 1 wherein the plurality of input signals comprise a plurality of clock signals.

Claim 3 (Original): The method of claim 2 wherein the plurality of clock signals are asynchronous relative to one another.

Claim 4 (Original): The method of claim 1 wherein preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state comprises:

performing a NOR operation on the other select signals to generate a NOR output; and

performing a NAND operation on the first of the select signals and the NOR output.

Claim 5 (Previously Presented): The method of claim 1 further comprising synchronizing the first of the select signals with a corresponding first of the input signals of the multiplexer prior to provide the first of the select signals to the multiplexer.

Claim 6 (Original): The method of claim 5 wherein synchronizing the first of the select signals comprises preventing the first of the select signals from reaching the multiplexer until after a rising edge and a falling edge of the first of the input signals.

Claim 7 (Original): A method for multiplexing signals comprising:

providing a plurality of select signals and a plurality of clock input signals for input by a multiplexer, each select signal adapted to cause the multiplexer to select a different one of the plurality of clock input signals for output by the multiplexer when the select signal is in a first logic state;

preventing a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state; and

preventing the first of the select signals from reaching the multiplexer until after a rising edge and a falling edge of a corresponding first of the clock input signals.

Claim 8 (Original): A multiplexer system comprising:

a multiplexer having:

a plurality of data input nodes adapted to receive a plurality of input signals;

an output node adapted to selectively output one of the plurality of input signals; and

a plurality of select nodes, each select node corresponding to a different one of the plurality of data input nodes and adapted to cause the multiplexer to select a different one of the plurality of input signals for output by the output node in response to a select signal of a first logic state being provided to the select node; and

selection circuitry coupled to the multiplexer and adapted to prevent a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state.

Claim 9 (Previously Presented): The multiplexer system of claim 8 wherein the plurality of input signals comprise a plurality of clock signals.

Claim 10 (Previously Presented): The multiplexer system of claim 8 wherein the selection circuitry comprises one-shot logic adapted to:

input a select signal for each select node of the multiplexer; and

determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state.

Claim 11 (Previously Presented): The multiplexer system of claim 10 wherein the selection circuitry further comprises synchronization logic coupled to the one-shot logic and the multiplexer and adapted to:

synchronize the select signal that is in the first logic state with a corresponding one of the input signals of the multiplexer; and

output the synchronized select signal to a respective select node of the multiplexer.

Claim 12 (Previously Presented): The multiplexer system of claim 10 wherein the selection circuitry further comprises decoder logic coupled to the one-shot logic and adapted to receiver a plurality of control signals and to generate each select signal based on the control signals.

Claim 13 (Previously Presented): The multiplexer system of claim 10 wherein the selection circuitry is adapted to:

perform a NOR operation on the other select signals to generate a NOR output; and

perform a NAND operation on the first of the select signals and the NOR output.

Claim 14 (Previously Presented): The multiplexer system of claim 10 further comprising synchronization logic adapted to synchronize the first of the select signals with a corresponding first of the input signals of the multiplexer before the first of the select signals is provided to the multiplexer.

Claim 15 (Previously Presented): The multiplexer system of claim 14 wherein synchronization logic is adapted to prevent the first of the select signals from reaching the multiplexer until after a rising edge and a falling edge of the first of the input signals.

Claim 16 (Original): A multiplexer system comprising:

a multiplexer having:

a plurality of data input nodes adapted to receive a plurality of input signals;

an output node adapted to selectively output one of the plurality of input signals; and

a plurality of select nodes, each select node corresponding to a different one of the plurality of data input nodes and adapted to cause the multiplexer to select a different one of the plurality of input signals for output by the output node in response to a select signal of a first logic state being provided to the select node; and

selection circuitry coupled to the multiplexer and adapted to:

prevent a first of the select signals that is in the first logic state from being provided to the multiplexer until the other select signals are in a second logic state; and

prevent the first of the select signals from reaching the multiplexer until after a rising edge and a falling edge of a corresponding first of the input signals of the multiplexer.

Claim 17 (Original): A multiplexer system comprising:

a multiplexer having:

a plurality of data input nodes adapted to receive a plurality of input signals;

an output node adapted to selectively output one of the plurality of input signals;

a plurality of select nodes, each select node corresponding to a different one of the plurality of data input nodes and adapted to select a different one of the plurality of input signals for output by the output node in response to a select signal of a first logic state being provided to the select node;

one-shot logic adapted to:

input a select signal for each select node of the multiplexer; and

determine if only one of the input select signals is in the first logic state, and if so, output at least the select signal that is in the first logic state; and

synchronization logic coupled to the one-shot logic and the multiplexer and adapted to:

synchronize the select signal that is in the first logic state output from the one-shot logic with a corresponding one of the input signals of the multiplexer; and

output the synchronized select signal to a respective select node of the multiplexer.